ABSTRACT OF THE DISCLOSURE

A first dynamic logic circuit has an output node on which a scan value is provided during scan. One of one or more second dynamic logic circuits has an input coupled to the output node of the first dynamic logic circuit, and an output of the second dynamic logic circuits is sampled in response to the scan value during scan. In one embodiment, clock generation circuitry may be included which generates a first clock, a second clock, and a third clock. At least one evaluate pulse on the first clock prior is generated prior to sampling the output of the second dynamic logic circuits, the first clock controlling at least the evaluation of the second dynamic logic circuits. The second and third clocks are generated to isolate the output node from inputs to the first dynamic logic circuit responsive to the scan mode signal indicating that scan is active.